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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,228	09/26/2003	Kuen-Suey Hou	BHT-3212-43	6830

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EXAMINER	
PSITOS, ARISTOTELIS M	
ART UNIT	PAPER NUMBER
2627	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/18/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,228	HOU, KUEN-SUEY	
	Examiner	Art Unit	
	Aristotelis M. Psitos	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response of 10/17/06 has been considered with the following results.

Specification

The amendment to the title of the invention is greatly appreciated, and has been entered.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

1. Claims 1,15 and 2,3, 13,14 and 16,17 are rejected under 35 U.S.C. 102(a) as being anticipated by the acknowledge prior art or alternatively under 35 USC 103 (a) as being unpatentable further in view of Chiba.

The identification as to the prior art as US 6614740 is greatly appreciated.

As recited in claim 1, the acknowledged prior art discriminates, using reflected signals from the header area of an optical disc, whether a plurality of headers are present.

The light beam-detecting module is inherently the described photodetector arrangement/segment/module in such prior art devices. The functional limitations present in lines 11-19 are interpreted as merely describing the operation thereof.

The signal-detecting module is inherently the appropriate circuitry that detects the signal (i.e., the rf component and subsequent signal processing segments) of the detected reflected light signal that is present in such prior art devices. The functional limitations of the ultimate wherein clause is interpreted as merely describing the operation thereof.

Under 102 considerations, the examiner concludes that the address mark signal is inherently present/generated – due to the slice level condition – applicants attention is further drawn to the description of the acknowledged prior art – US 6614740 starting at col. 4 line 36 till col. 9 line 56.

Alternatively under 103 considerations, if applicant can convince the examiner that no address mark signal is generated, then under 103 considerations, the examiner relies upon the further teaching from Chiba to further modify the acknowledged prior art.

It would have been obvious to modify the base system of Park et al/the acknowledged prior art with the teaching from Chiba, motivation is to use the address mark signal in lieu of the slice level value in order to detect the address marks.

The limitations of the analogous method claim 15 are met when such prior art system(s) operate.

With respect to claims 2,3 and analogous method dependent claims 16 & 17, the acknowledged prior art to Park et al discloses in this environment, the ability of having/generating a "header" mask signal – see the discussion of figure 7 starting at col. 8 line 65. The examiner interprets this "header" mask signal as the claimed mask signal.

With respect to claims 13 and 14, the use of logical gates, i.e., "and", "or", "nand", etc. in electronic logic circuitry – which the examiner interprets as the claimed logical unit, is well known and Official notice is taken thereof. Use of such in electronic circuitry for their inherent capabilities is motivation to use such with Park et al to yield a more accurate/stabilized servo system.

Response to Arguments

2. Applicant's arguments filed 11/17/06 have been fully considered but they are not persuasive & or are not persuasive due to the new ground(s) of rejection.

Applicant's argues against the rejection predicated upon

a) there is no address mark

b) the claimed required continuous received address mark and the first and second header signals.

As indicated above, the examiner interprets the slice level as providing/meeting the address mark signal. Since as disclosed in the acknowledged prior art, such a level is set/established to ensure proper recognition of the address mark signal area. That the signals are continuously read, such is present – see the description of figure 9 of the acknowledged prior art.

Alternatively, as further described by Chiba, the address mark is present in this environment prior to the header signals – to indicate the presence of the header signals. Furthermore, such signals must be read continuously else the header region/signals would not be read.

3. Claims 4,5,6,7,8,9, 10, 11,12, 18,19,20,2122,23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the art as applied to claim 3 above, and further in view of either JP 2002-083461 or Gulick et al.

With respect to claims 4 and 12 there is no clear depiction of a "counter" in the combined system as relied upon above in paragraph 2.

The ability of using "counters" for the inherent ability of counting pulses is taught by either the JP system – see the discussion starting at paragraph 23 of the MAT (Machine assisted translation) of the JP document, or Gulick et al.

It would have been obvious to modify the base system as relied upon above in paragraph 2 with the above additional counters teaching from either JP 2002-083461 or Gulick et al, motivation is to provide for an accurate mask signal duration predicated upon a count value.

With respect to claim 5, counters normally count in bytes/bits starting at a value of "0". The examiner considers the limitations of claim 5 as inherently present in either of the secondary references.

With respect to claim 6, "the gap" is not understood. If this language is attempting to define that section in a header region, then such is inherently found in the acknowledged prior art.

With respect to claims 7-11, 18-13, these limitations merely describe the operation of the hardware and in method terminology of their parent claims. Since the examiner has met the

hardware/apparatus limitations as noted above in paragraph 2, these functional limitations follow and are met.

Response to Arguments

Applicant's arguments filed 11/17/06 have been fully considered but they are not persuasive. See the reasons with respect to the parent claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristotelis M. Psitos whose telephone number is (571) 272-7594. The examiner can normally be reached on M-F: 6:00 - 2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dwayne D. Bost can be reached on (571) 272-7023. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aristotelis M Psitos
Primary Examiner
Art Unit 2627

AMP